



Stress and Reliability for 3D Interconnects

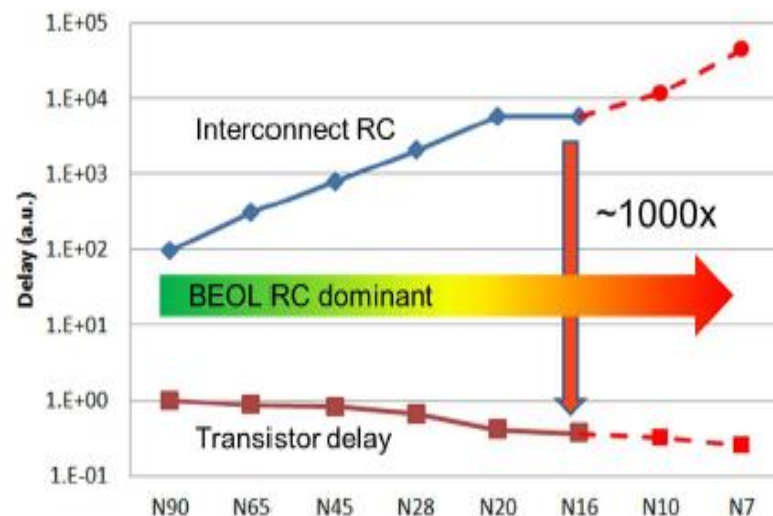
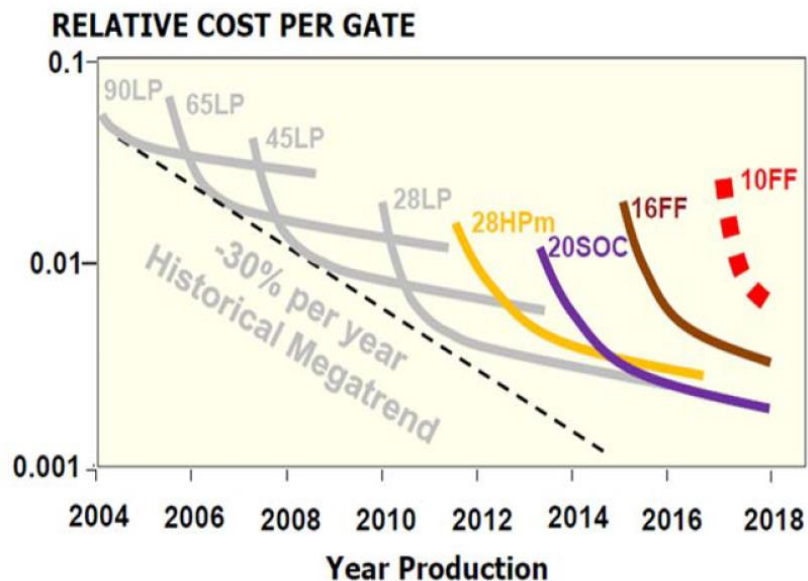
**Tengfei Jiang, Jay Im, Rui Huang
and Paul S. Ho**

The University of Texas at Austin

FCMN 2015, Dresden

CMOS and BEOL Scaling Challenges

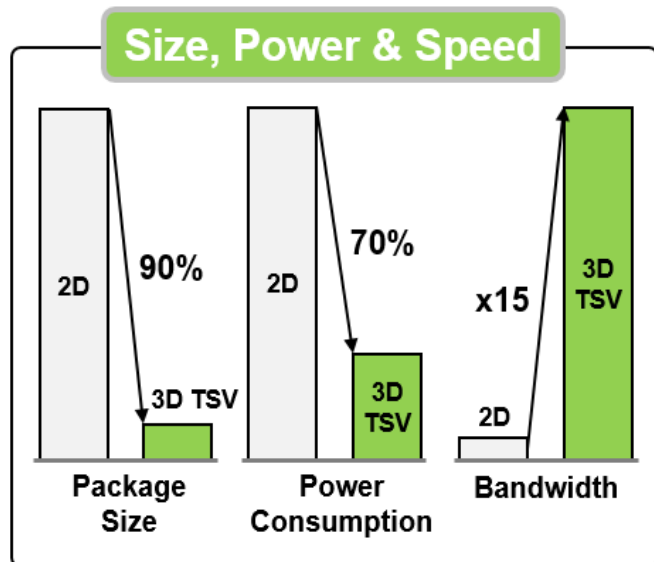
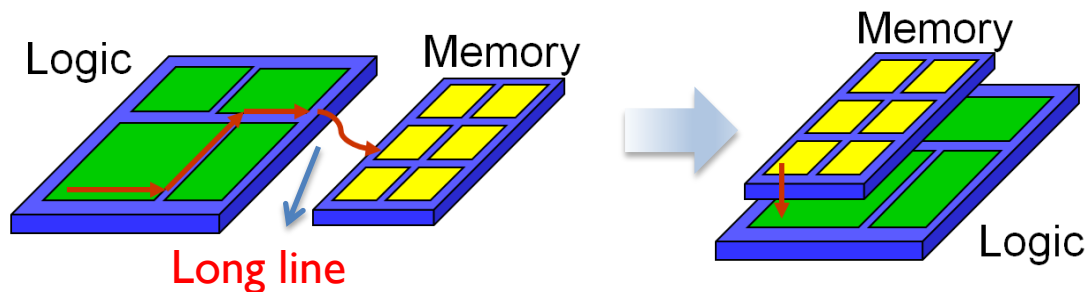
- Conventional CMOS scaling continues
 - More difficult
 - More expensive
- Interconnects dominating chip energy and performance, not transistors!



Source: Qualcomm

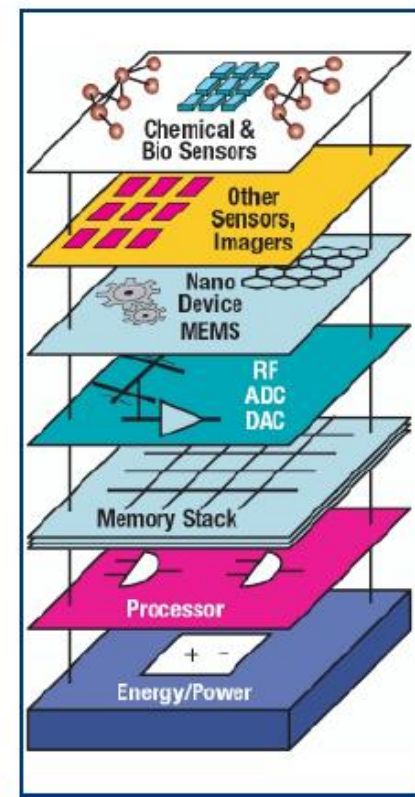
Benefits of 3D Integration

- Solution for mobile system and bandwidth requirement



Source: Micron

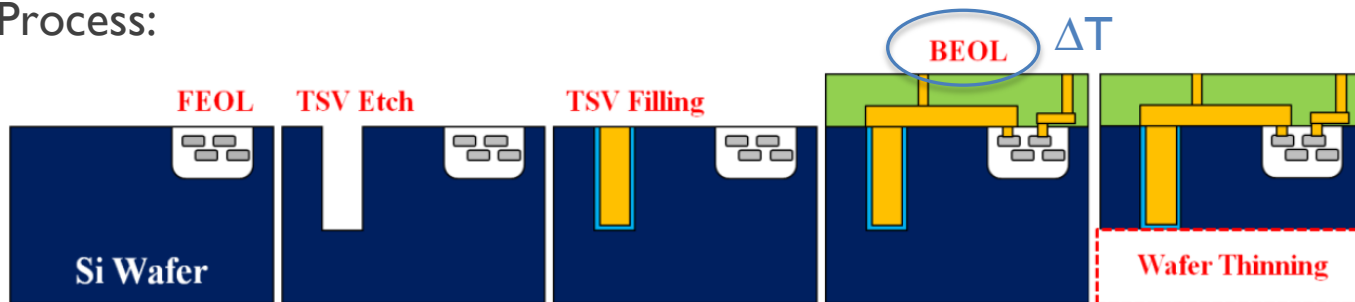
- Smaller form factor
- Better performance
- Lower power consumption
- Wider bandwidth
- Lower cost
- Heterogeneous integration



Lu et al., 2007

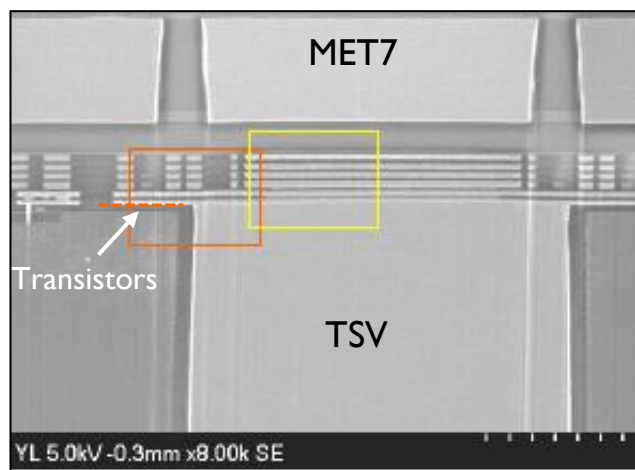
Thermo-Mechanical Reliability for 3D Integration

- Via Middle Process:

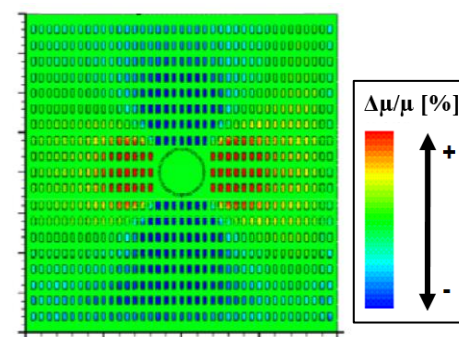
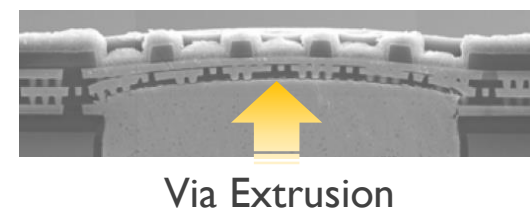
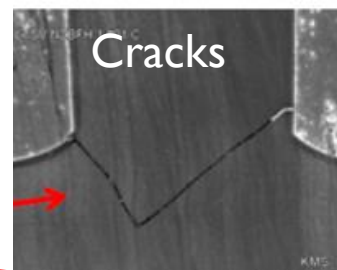
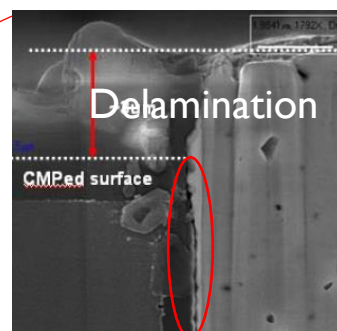


- CTE mismatch: thermal stress in/around Cu TSV.

- $\alpha_{Cu} = 17 \text{ ppm/K}$, $\alpha_{Si} = 2.3 \text{ ppm/K}$



Source: TI, Samsung, Qualcomm



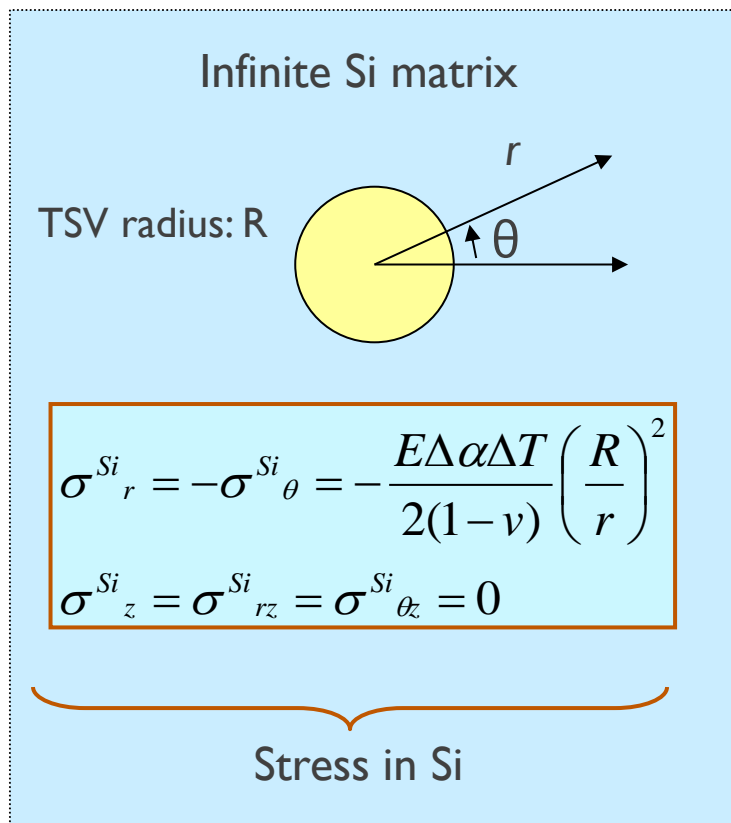
Mobility Change



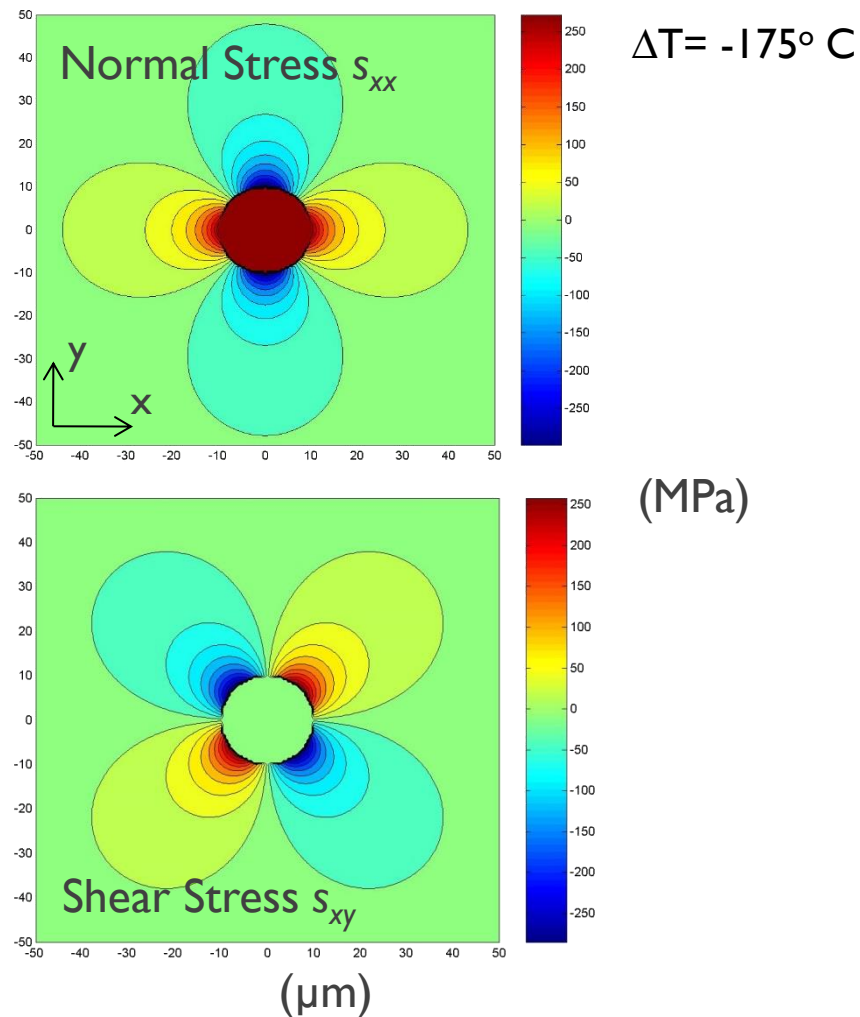
Outline

- Thermo-mechanical Reliability of TSVs
 - TSV Stress Characteristics
 - Local Plasticity and Via Extrusion
- Effect of Microstructure and Extrusion Statistics
- Synchrotron study of die-stack structures
- An Approach to Reduce Via Extrusion

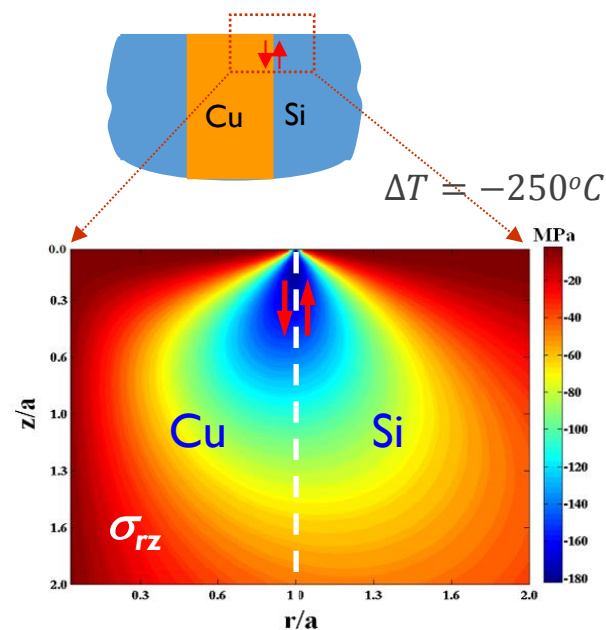
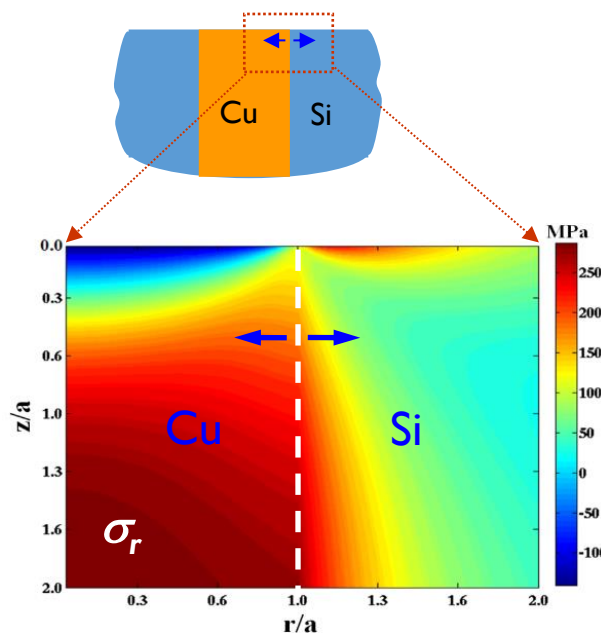
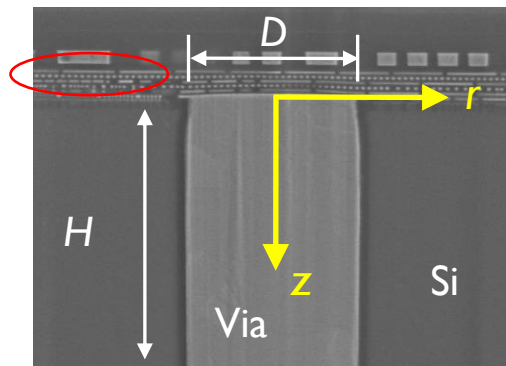
2D Stress Solution of Single TSV



- 2D stresses controlled by CTE mismatch between Cu and Si.



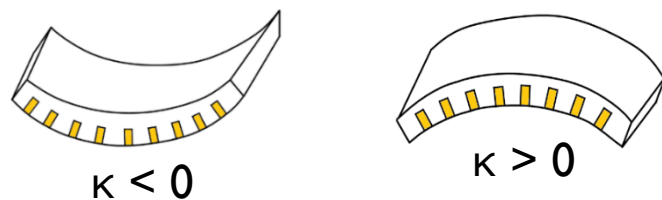
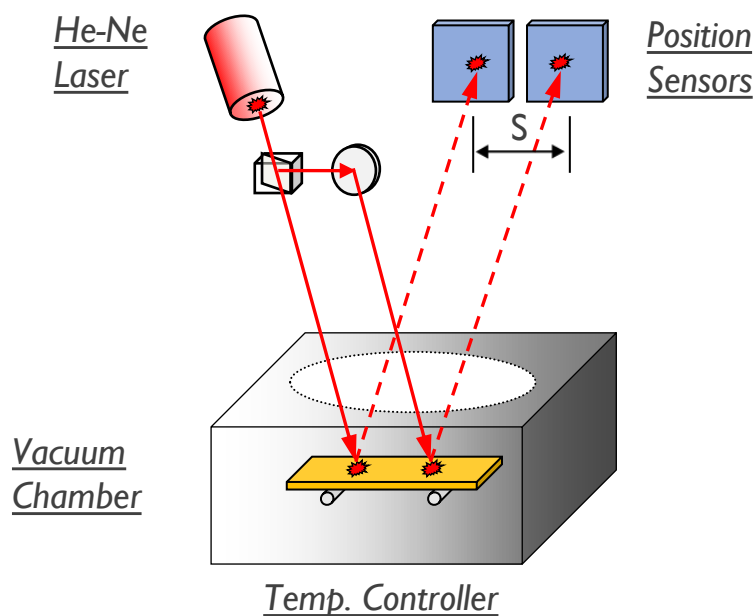
Tri-Axial Stress State and Near Surface Stress



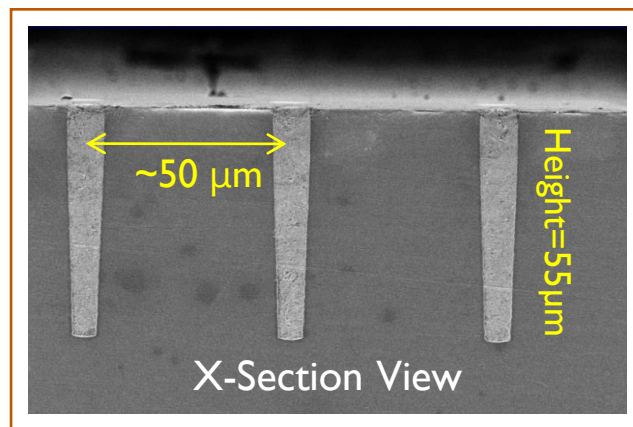
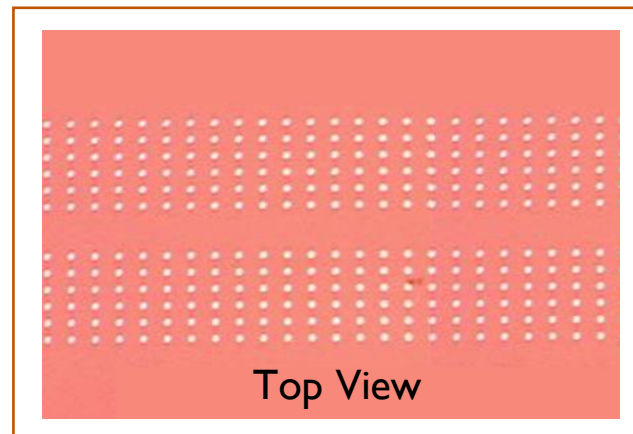
- TSV confined by surrounding Si – distinct characteristics.
- Stress and materials characterization
 - Substrate curvature, μ -Raman.
 - EBSD, TOF-SIMS, Nanoindentation, Synchrotron x-ray microdiffraction.

Thermo-Mechanical Behavior of TSVs

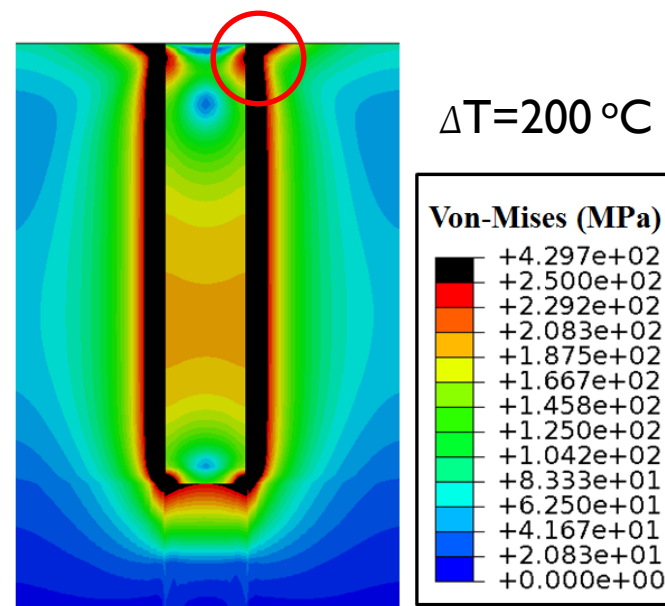
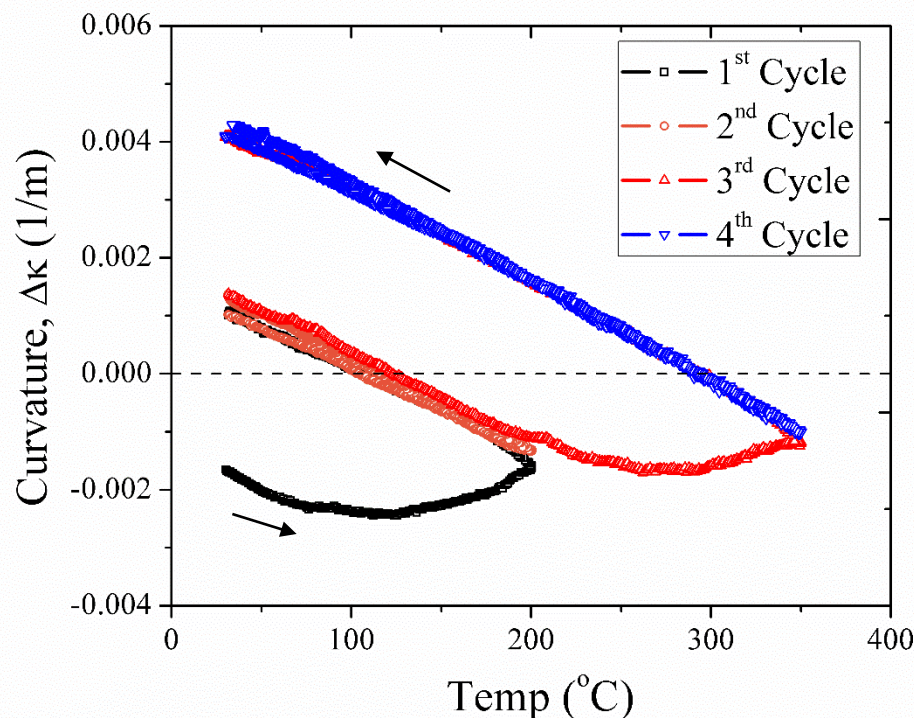
- In situ* measurement of material behaviors during thermal cycling.



$$\alpha_{\text{Cu}} = 17 \text{ ppm/K}, \alpha_{\text{Si}} = 2.3 \text{ ppm/K}$$



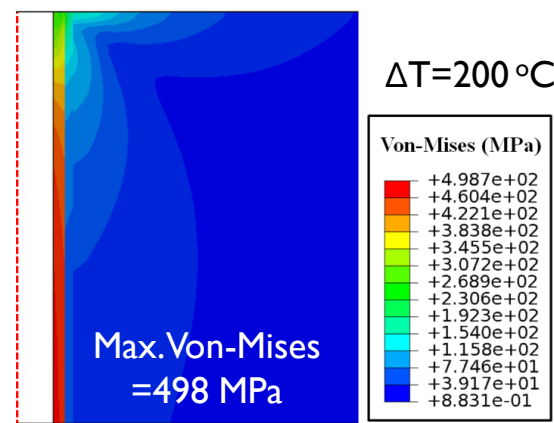
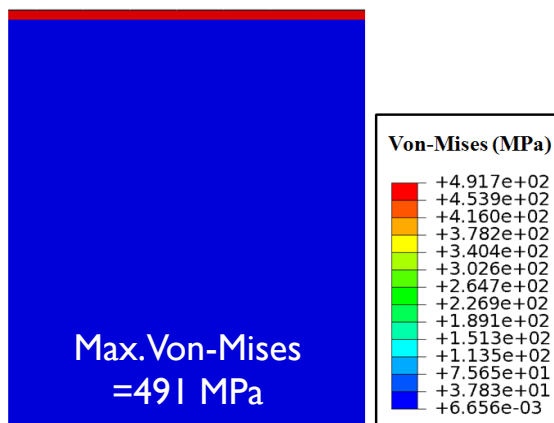
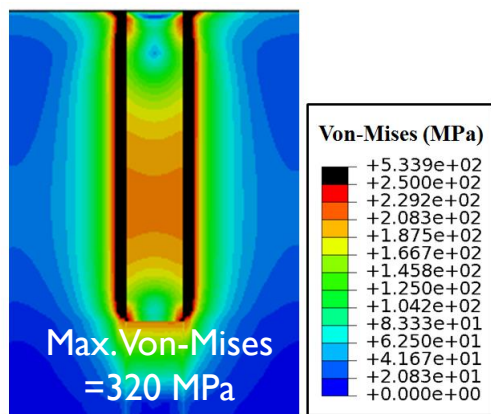
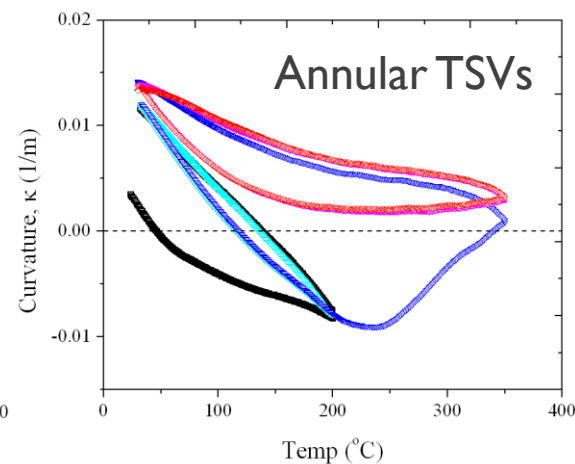
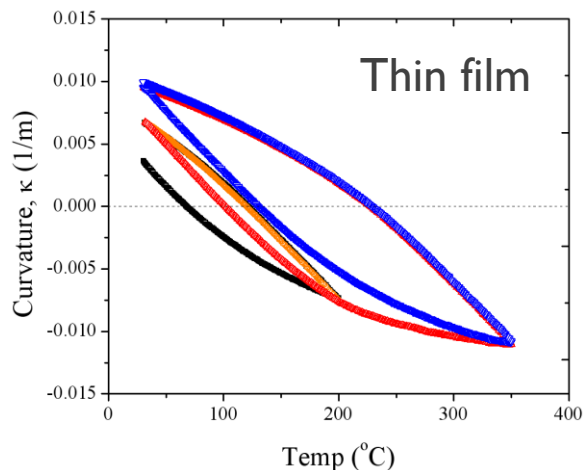
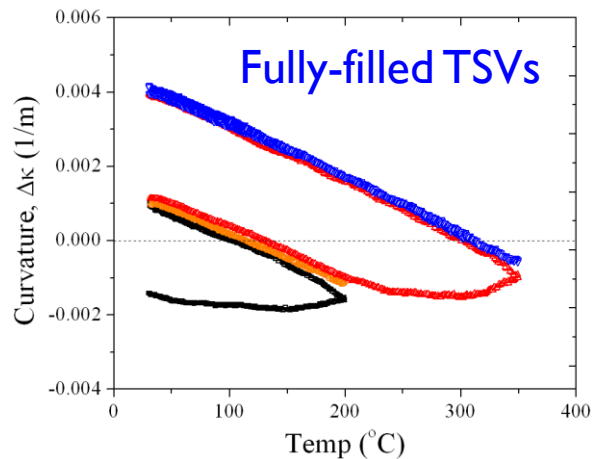
Curvature-Temperature Behavior of TSVs



Localized plasticity

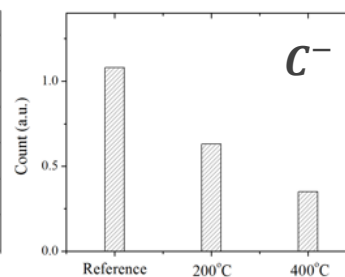
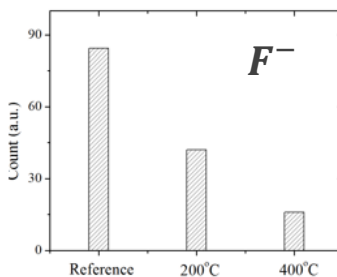
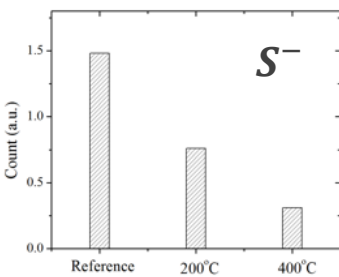
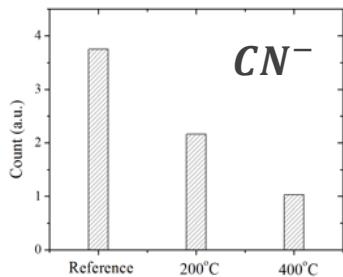
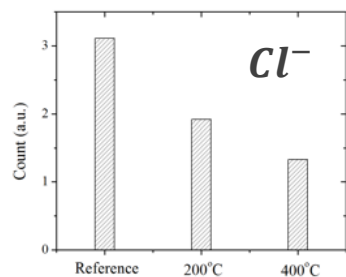
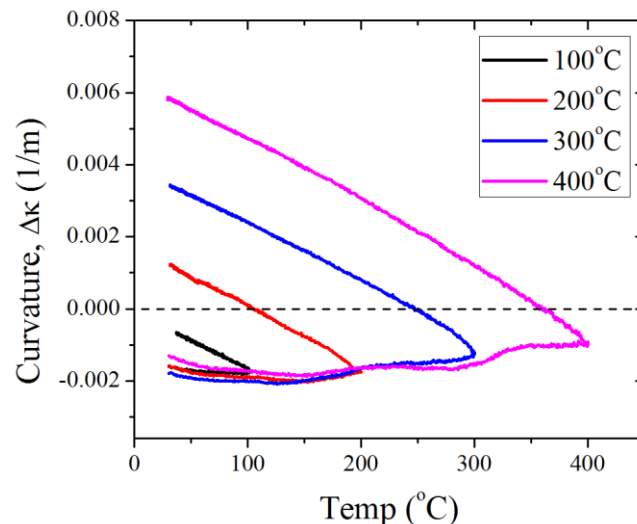
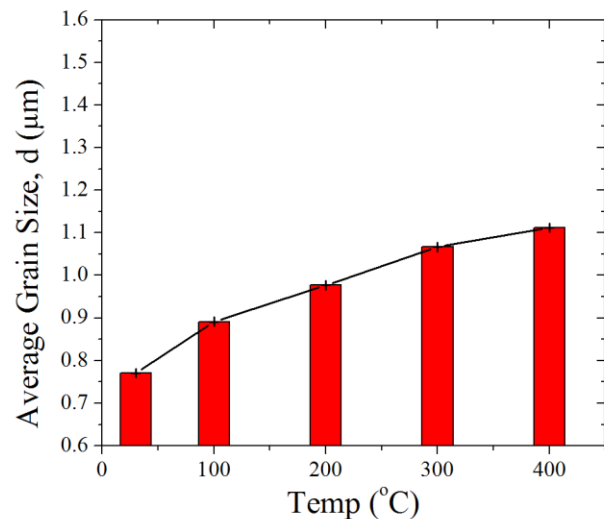
- Nonlinear behavior in heating, linear behavior during cooling.
- Stress-free temperature determined.
- Tri-axial stress state - local plasticity.

TSV Curvature Behavior: Tri-axial Stress State


 $\Delta T = 200^\circ\text{C}$

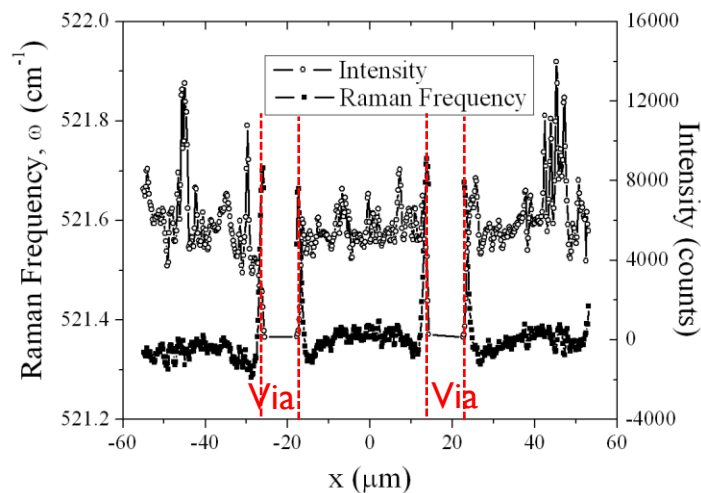
- TSV stress increased with thermal cycling \rightarrow residual stress.

Microstructure Evolution and Stress Accumulation



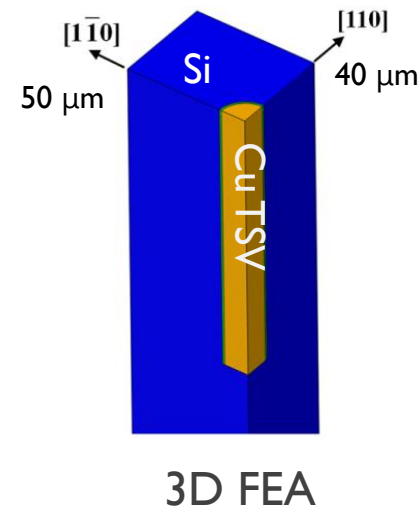
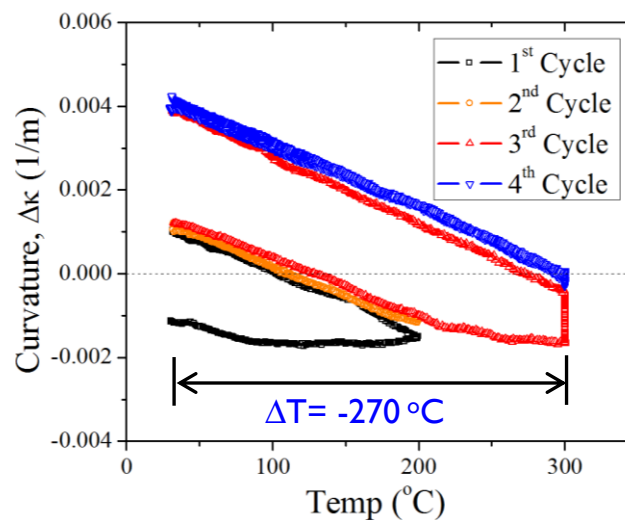
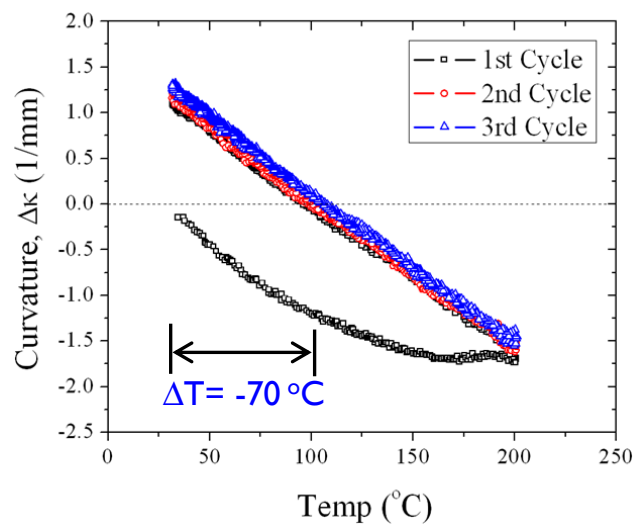
- Out-diffusion of additives during grain growth.
- Grain growth → accumulation of residual stress.

Correlation with Micro-Raman

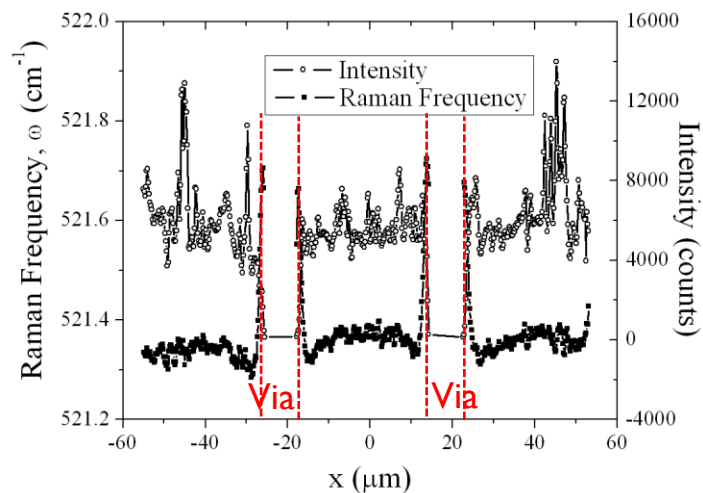


- Strain in Si \rightarrow Raman frequency change.

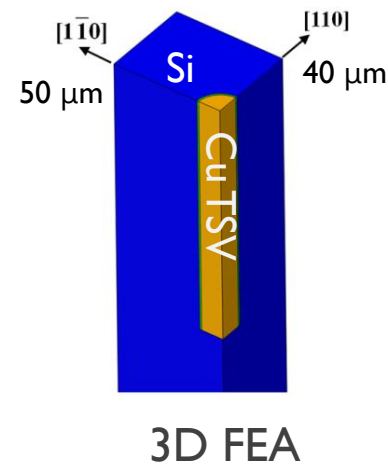
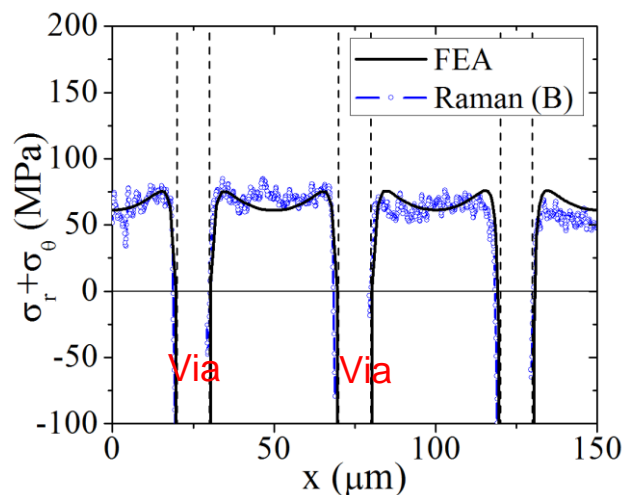
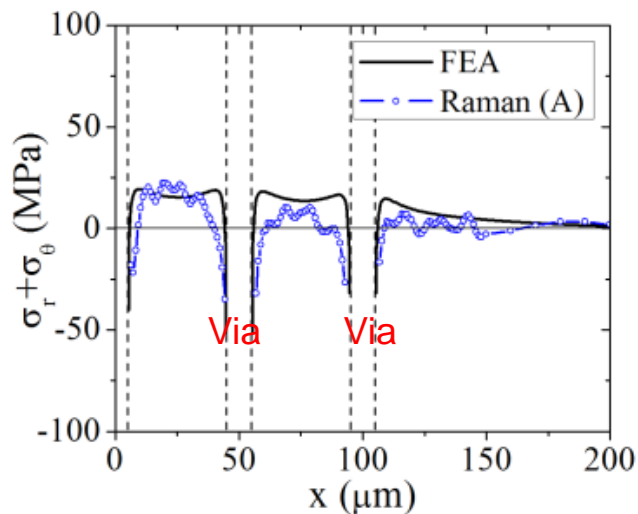
$$\sigma_r + \sigma_\theta \text{ (MPa)} = -470\Delta\omega_3 \text{ (cm}^{-1}\text{)}$$
- Annealing reset stress-free temperature.
- Change of residual stress at RT.
- Correlation by FEA.



Correlation with Micro-Raman

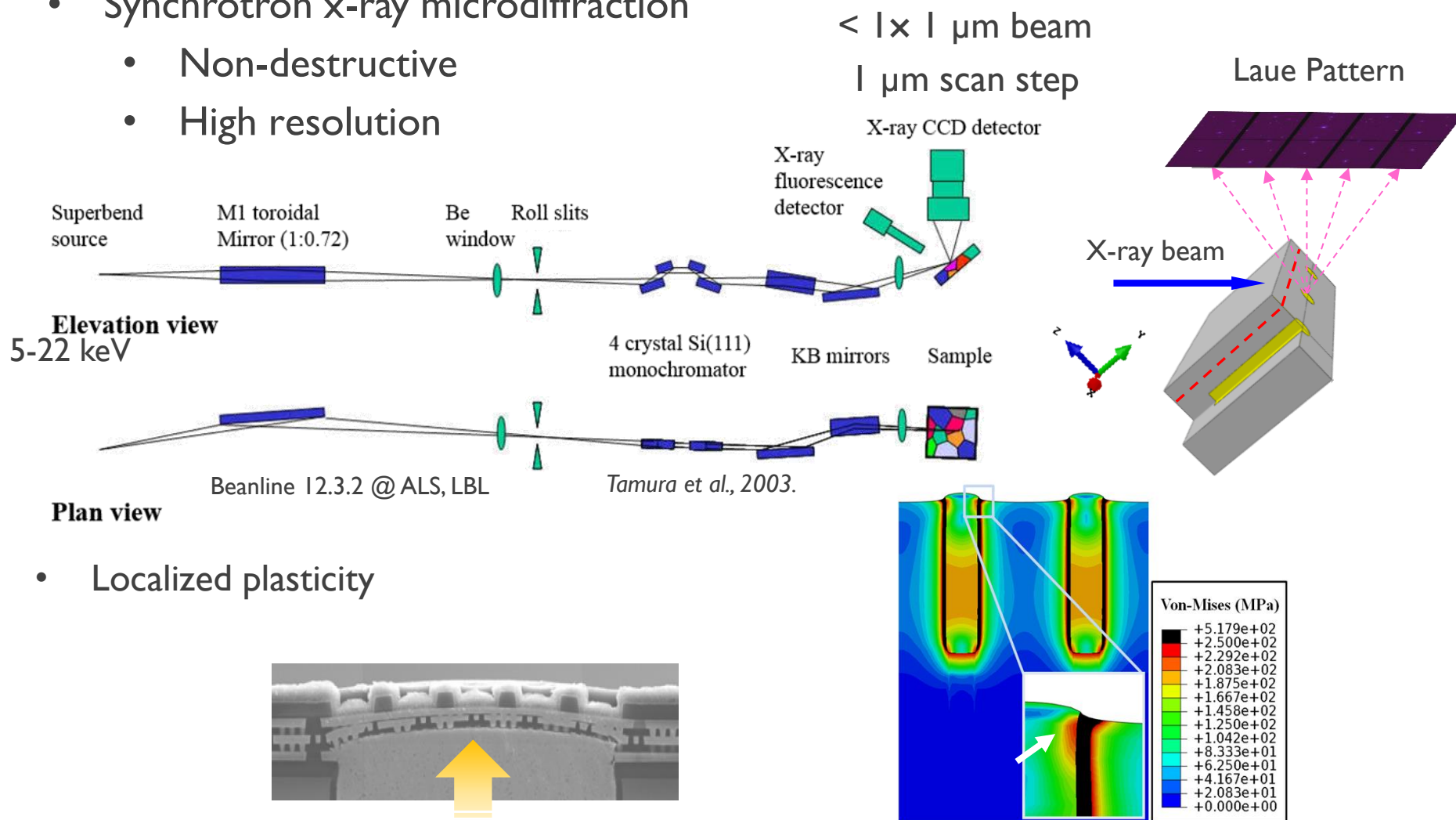


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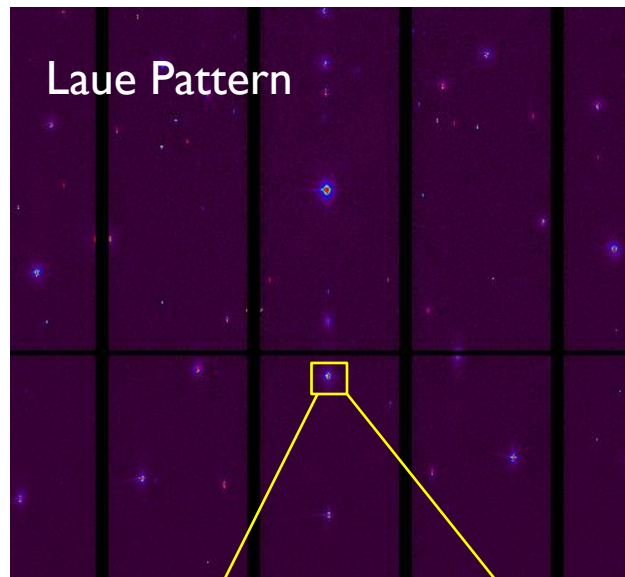


Local Plasticity and Via Extrusion

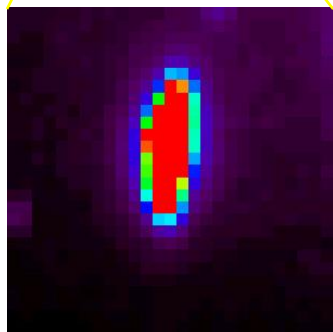
- Synchrotron x-ray microdiffraction
 - Non-destructive
 - High resolution



White Beam Scanning X-ray Microdiffraction (μ SXRD)

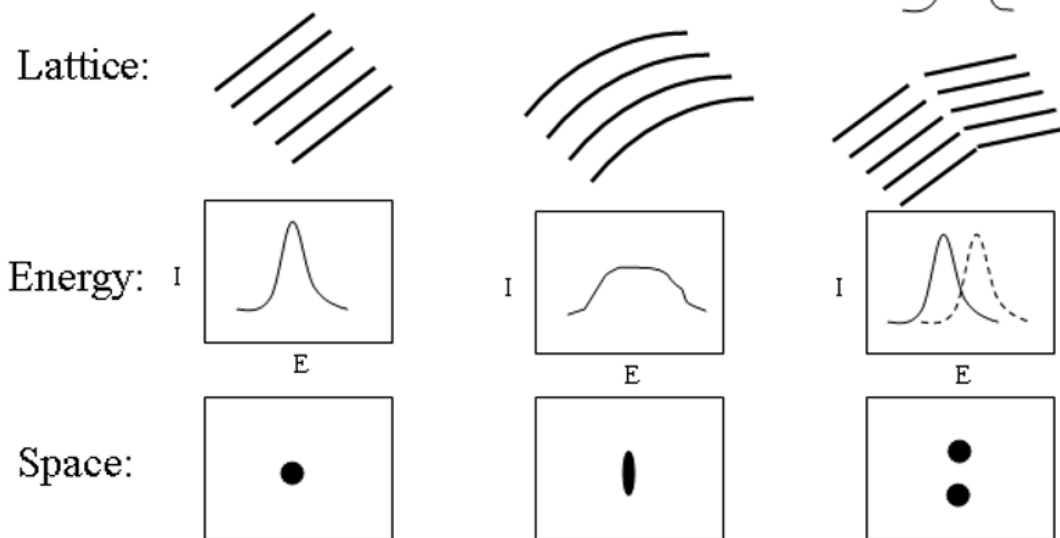


Laue Peak



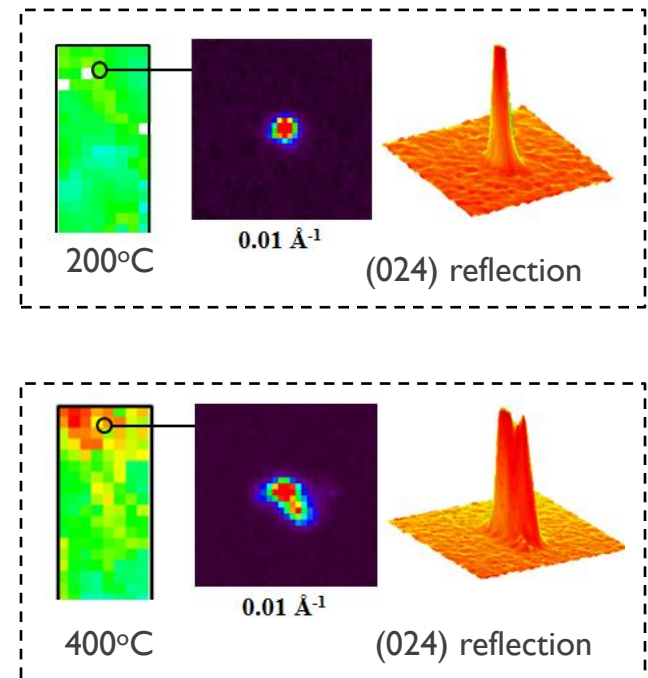
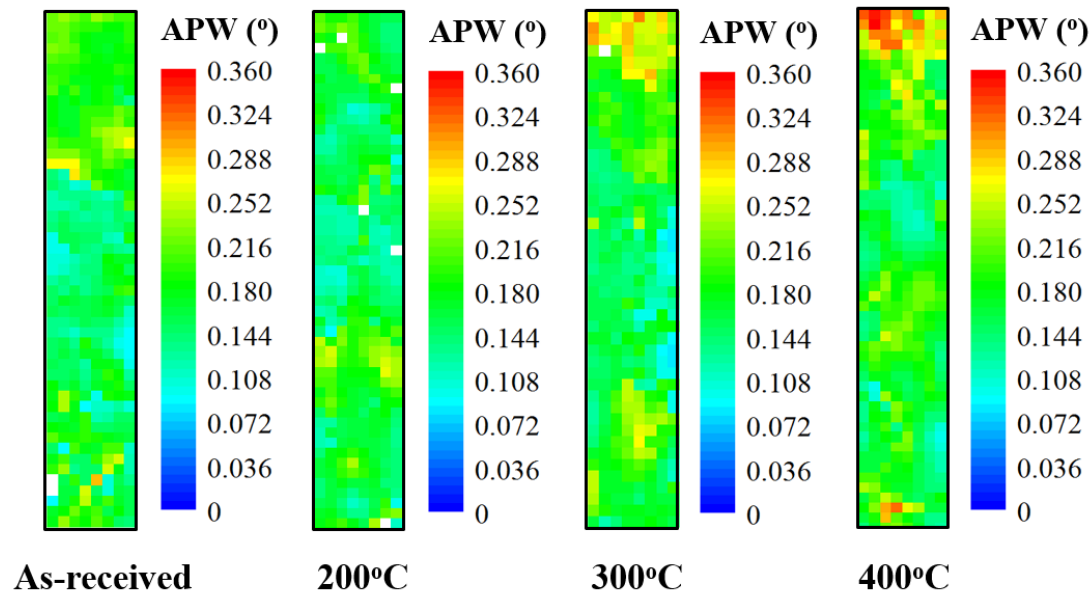
- Peak shapes provide information on plastic deformation and dislocation distribution in the diffracted volume.

$$n\lambda = 2d_{hkl}\sin\theta$$



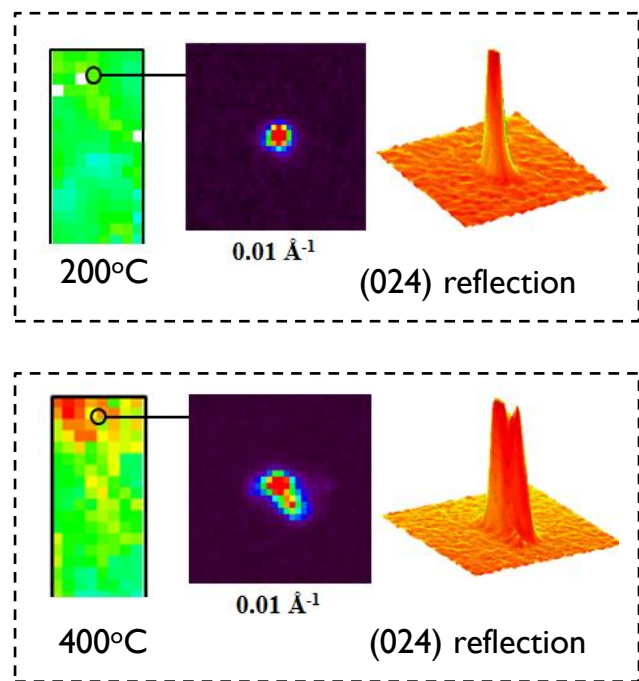
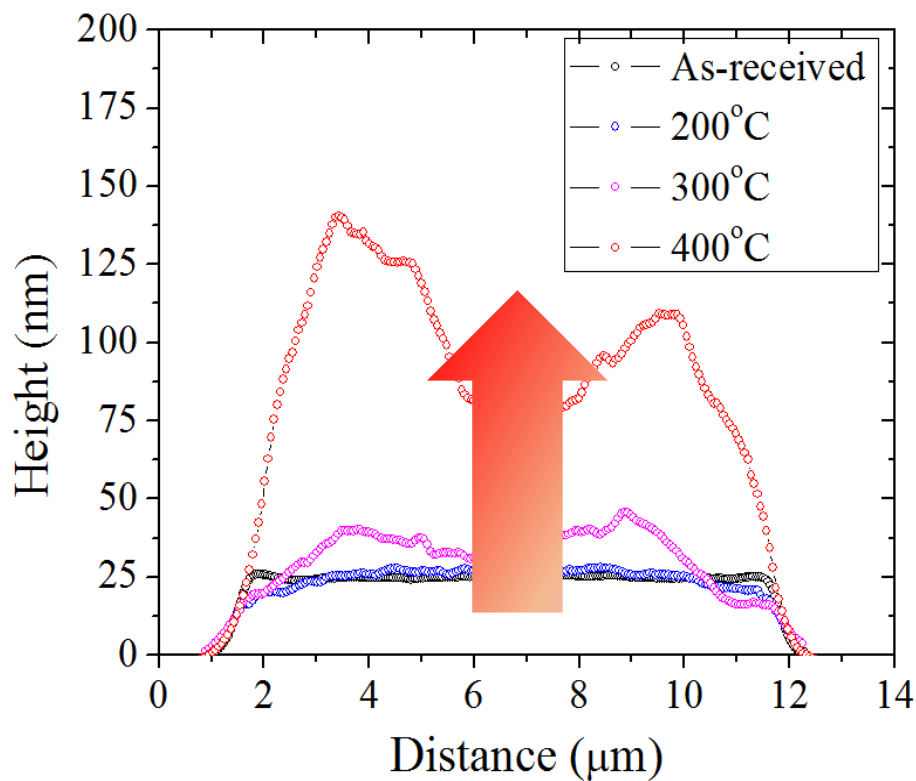
Tamura, 2008.

Local Plasticity in TSVs



- Average peak width (APW): peak broadening.
- Local plasticity near top of TSV.

Via Extrusion

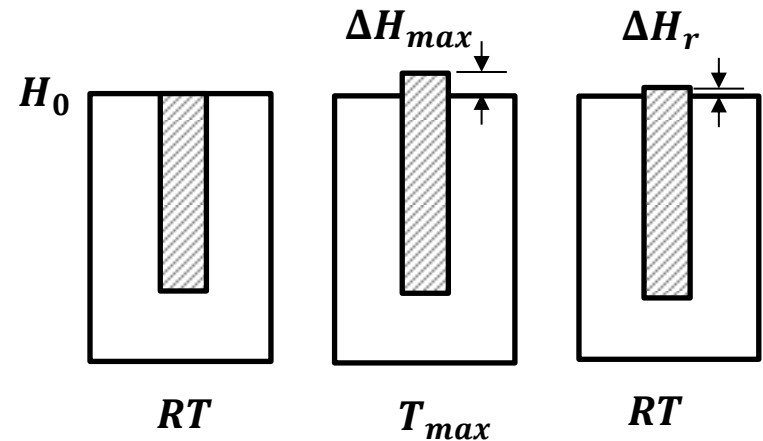
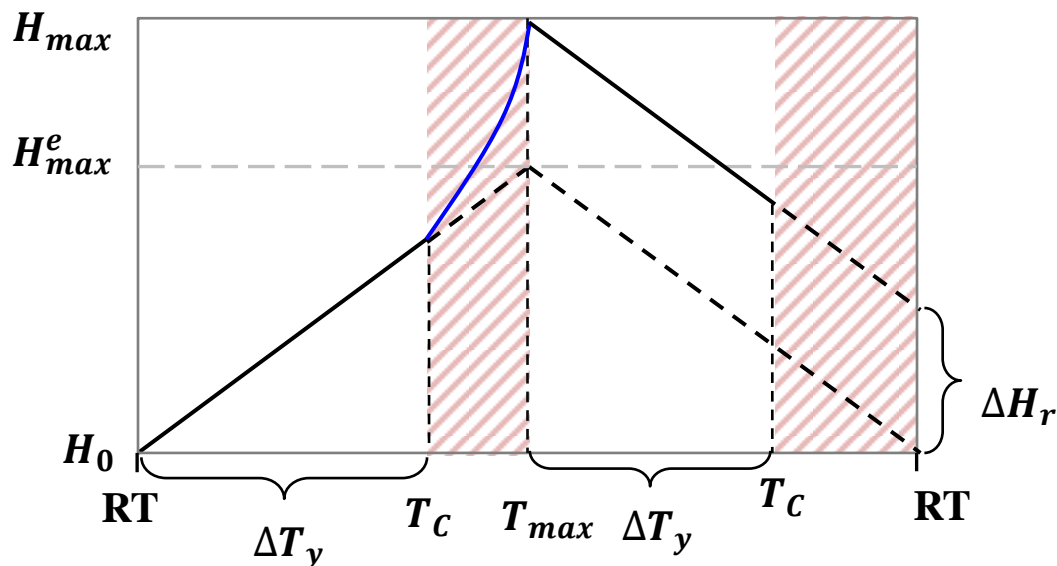


- Via extrusion show correlation to local plasticity (APW).

Via Extrusion

- Irrecoverable deformation → Via extrusion

- Grain growth (indirect)
- Dislocation glide
- Diffusional creep



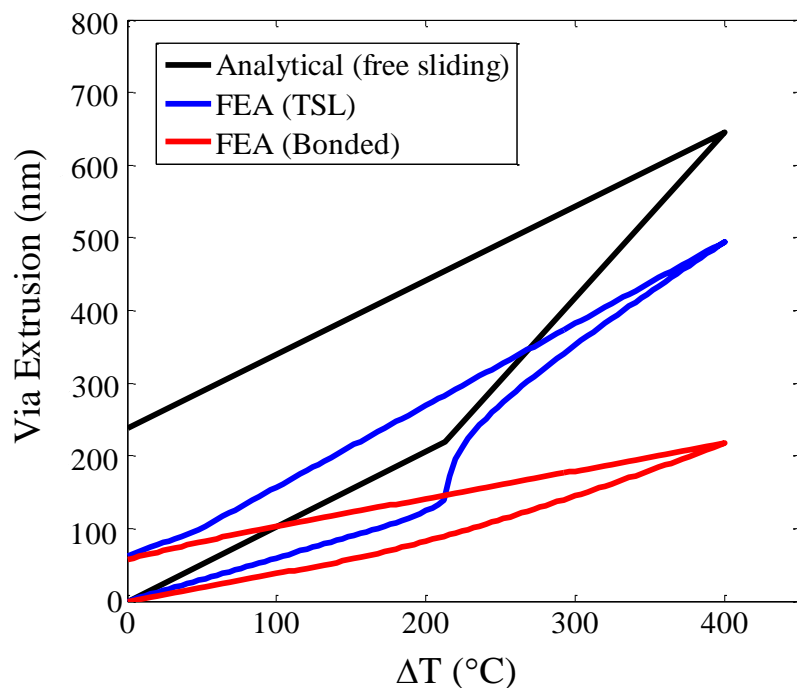
$$\alpha_{Cu} > \alpha_{Si}$$

$$\Delta H_r = \Delta H_p - \Delta H_e = H(\beta_p - \beta_e)(\Delta T_m - \Delta T_y)$$

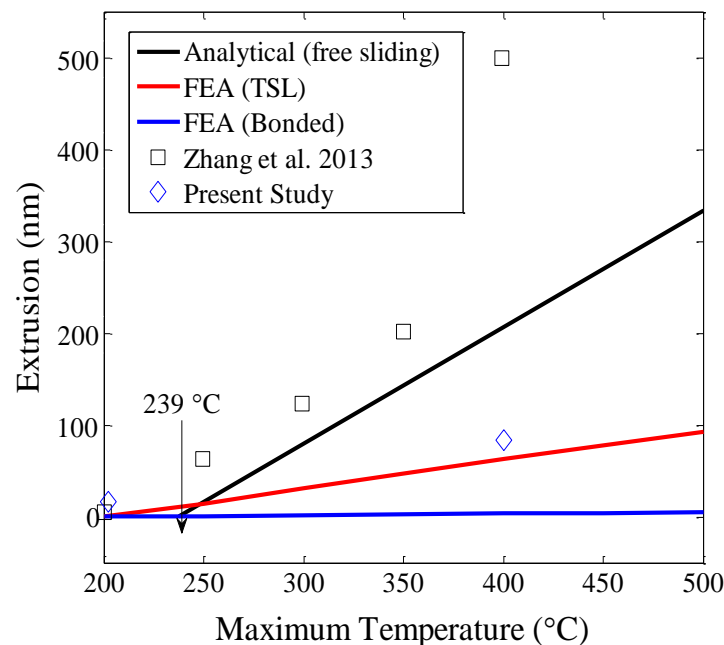
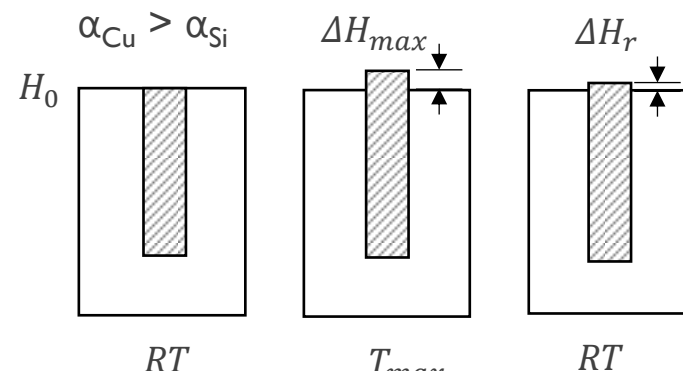
- High T: mass transport occurred.
- Low T: plasticity occurred.

- In situ measurement to elucidate inelastic process.

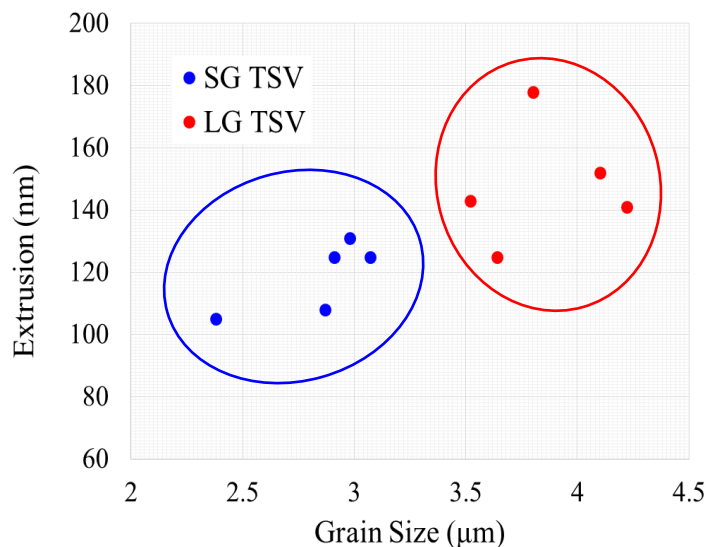
Modeling of Extrusion



- Via extrusion increases with T_{max} (beyond a critical T).
- Increasing yield strength of Cu and interfacial adhesion would help reduce via extrusion.

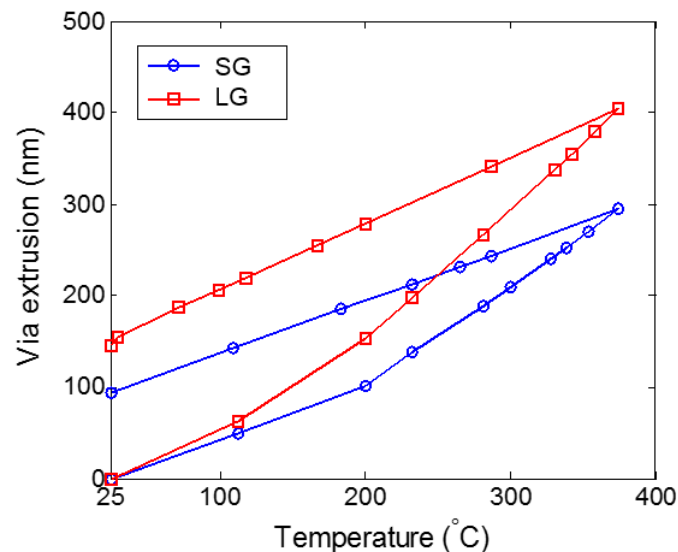
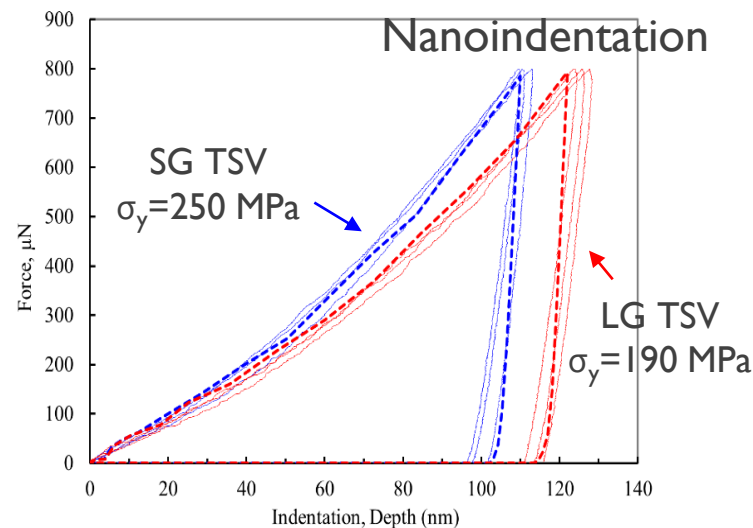


Material Property-Extrusion



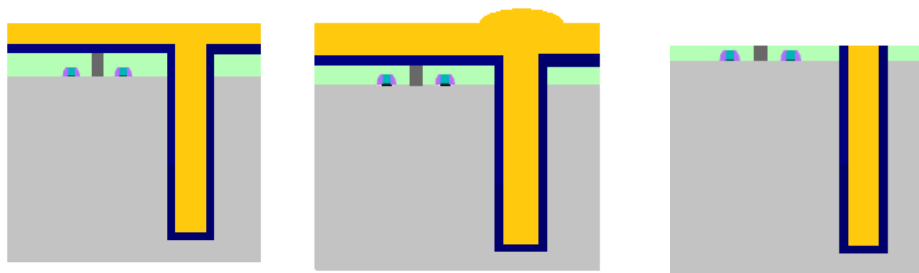
$$\sigma_y = \sigma_o + \frac{k_y}{\sqrt{d}}$$

- Controlling the Cu grain size to reduce via extrusion by optimizing the post-plating anneal.



Statistics of Via Extrusion

- Post-plating (pre-CMP) annealing introduced in via-middle process



Via Filling

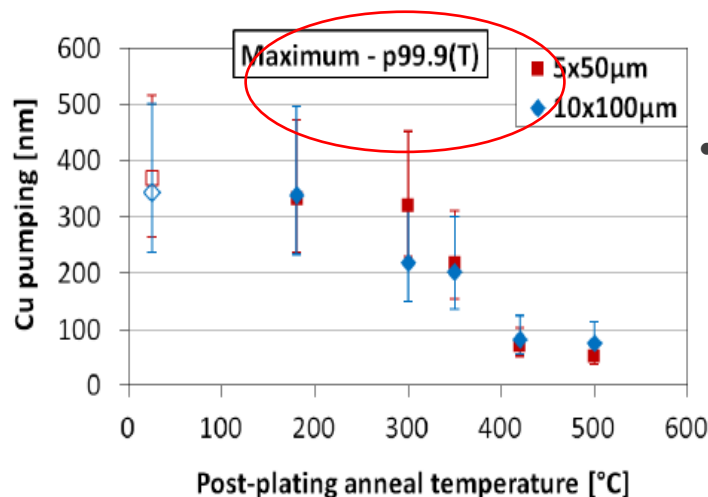
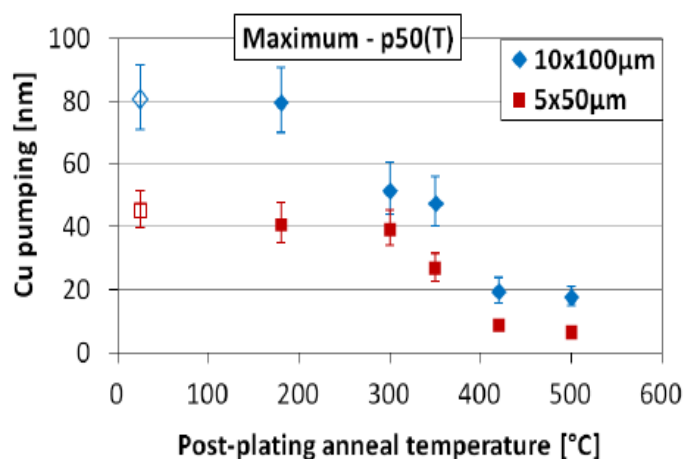


Anneal



CMP

- Improve extrusion by stabilizing grain structure and stress state.
- Not effective in statistics of extrusion (weakest link).
- Grain structure near via top and diffusion.

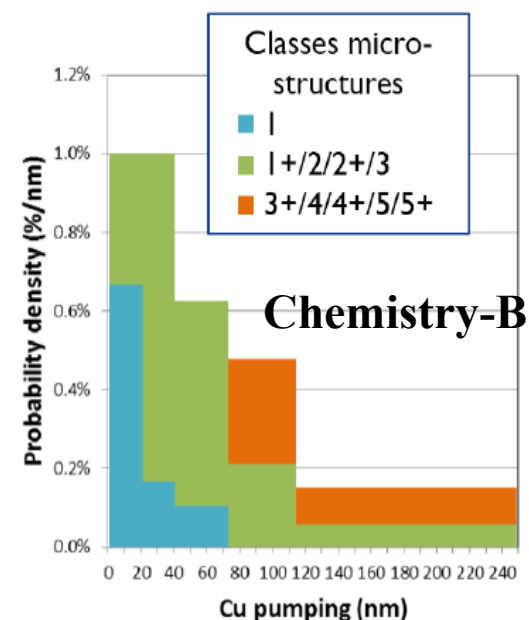
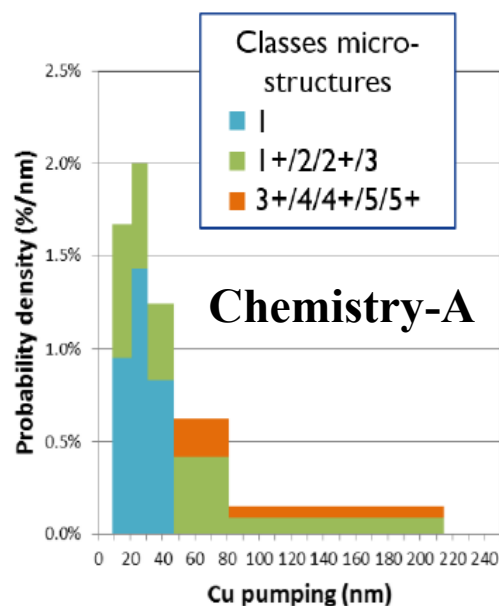
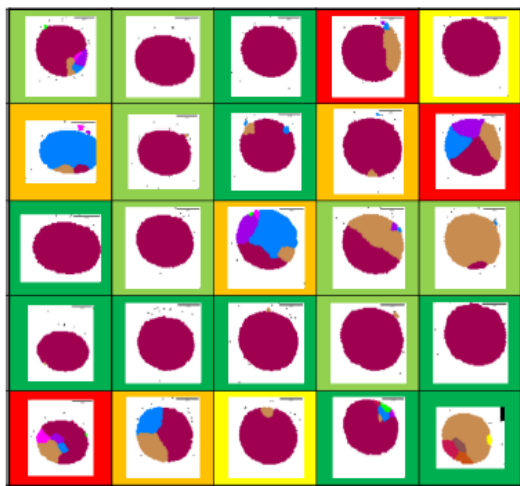


- Largest extrusion (0.1%) determine BEOL integrity and reliability

De Messemaeker et al., 2013, 2014

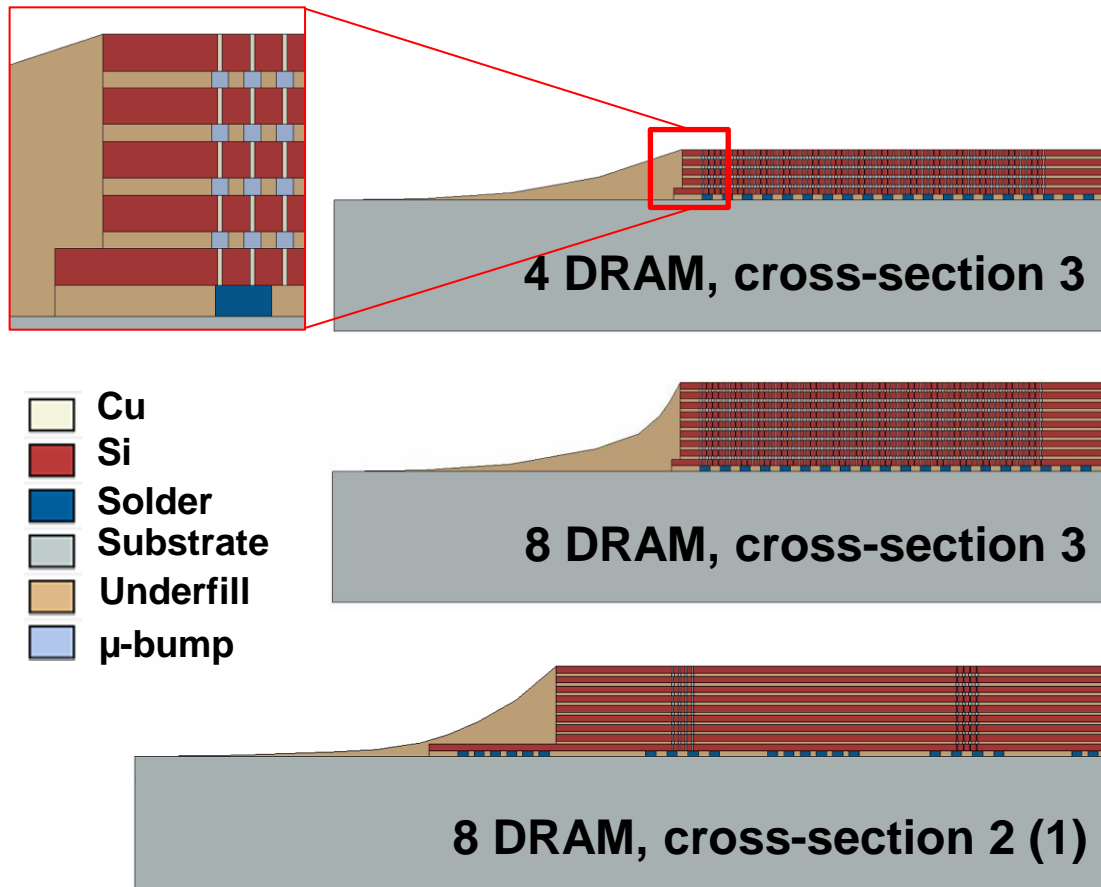
Grain Structure Effect on Via Extrusion

- Suppress diffusion (Interface, grain boundary)
 - Good adhesion at the interface. (via etch, oxide/liner/seed)
 - Twin boundary.



- Cannot **reduce distribution due** to the worst case.
- The weakest link in statistic distribution important.

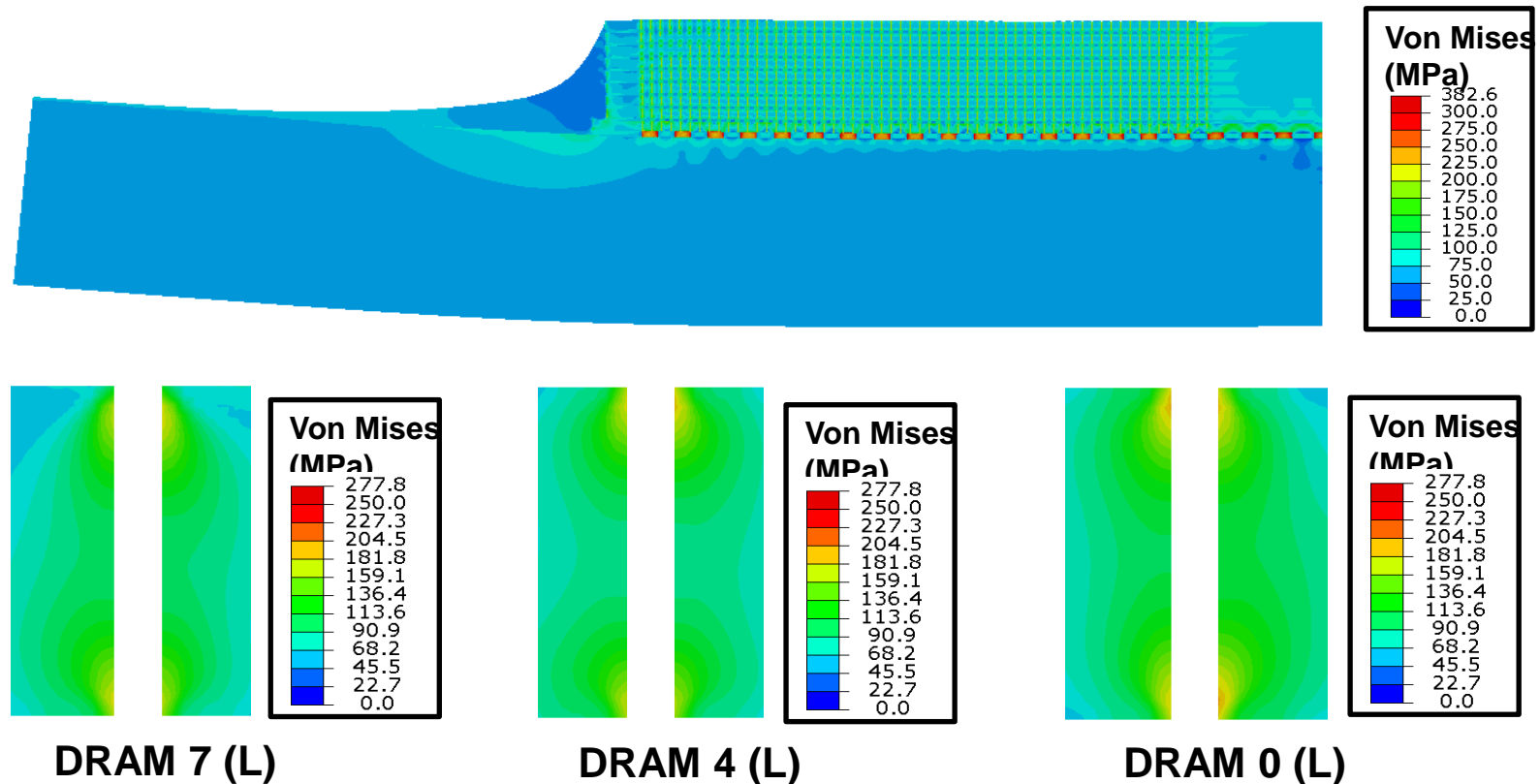
FEA of Die Stacks



- 2D plane strain FEA model
 - Symmetry at package center
 - fix bottom right corner.
 - Solder bump placement is approximated
- Consider die stacking process
 - Substrate: 100°C-RT
 - Chip: 210°C-RT
- Underfill cure: 160°C-RT

Components	Initial Step -I
Si/TSV/ μ -bump/Solder	210°C 25°C
Underfill	160°C 25°C
Substrate	100°C 25°C

FEA vs Experiments



- FEA shows Von Mises stress increase from top to bottom (DRAM7 to DRAM 0)
- Trend from FEA is consistent with measurement, but the stress magnitude is smaller.
- FEA is underestimating stress level and the crack driving ERR.

Summary

- TSV characterized by substrate curvature, μ -Raman, EBSD, TOF-SIMS, Nanoindentation, synchrotron x-ray microdiffraction.
- TSV stress characteristics
 - Tri-axial stress state.
 - Accumulation of residual stress with grain growth and increased T.
 - Localized plasticity.
- Via extrusion
 - Local plasticity mechanism.
 - Cap layer to reduce extrusion.



Acknowledgements



- UT Interconnect and Packaging Group
- PI: Prof. Paul S. Ho
- Collaborator: Prof. Rui Huang



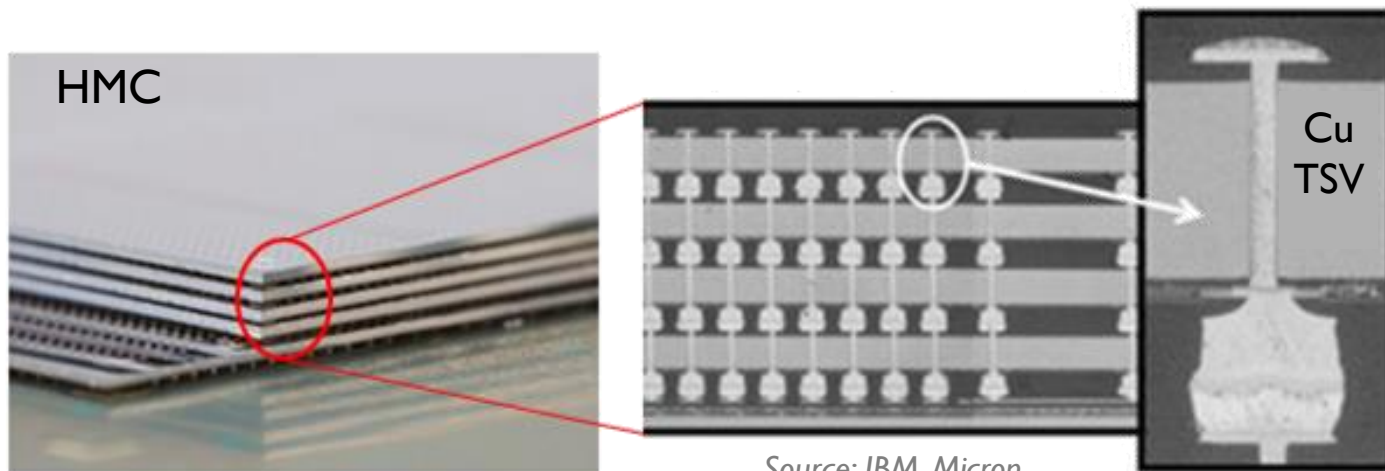


Thank you!



Through-Silicon Via (TSV)-based 3D Integration

- Stacking chips in z direction.



- Through-silicon via (TSV): vertical interconnection between stacked dies